What is claimed is;

1. A semiconductor circuit wherein a JTAG control circuit controlled by the security bit of a flash ROM is equipped between the JTAG port and a TAP (Test Access Port).

2. A semiconductor circuit comprising: an inhibit (INHIBIT) NAND gate;

a Pin scramble-circuit decoding a micro controller general-purpose port, which are set between the security bit of a flash ROM and the JTAG control circuit; and

a circuit wherein the inverted level of the one of the Pin scramble-circuit output is input the one side of the inhibit NAND gate and the output of the security bit of a flash ROM is input the other side of the inhibit NAND gate.

3. A semiconductor circuit comprising: an inhibit NAND gate;

a debug enable (DBG_EN) register as an internal register of the micro controller, which are set between the security bit of a flash ROM and the JTAG control circuit; and

a circuit wherein the inverted level of the one of the debug enable register output is input the one side of the inhibit NAND gate and the output of the security bit of a flash ROM is input the other side of the inhibit NAND gate.

4. A semiconductor circuit having a security releasing means comparing the data which is input a test port with the data stored in a memory device and turning on a switch when the two data agree,

the semiconductor circuit comprising: a memory device to store a control program and data;

a central processing unit to execute a specific process according to the program;

a test port to input and output test signals; and

a switch to control on/off between the test port and the memory device and/or the central processing unit according to the security bit set in a nonvolatile register.

5. A semiconductor circuit according to claim 4 wherein the security releasing means comprising: an address register keeping the address information input from the test port and specifying the memory range of the memory device;

a data register keeping the data information input from the test port;

a comparator comparing the data read out from the memory device based on the address information with the data kept in the data register; and

a logic gate turning on a switch when the two data agree, independent of the state of security bit.

6. A semiconductor circuit according to the claim 4 wherein the security releasing means comprising: an address counter counting the timing information input from the test port sequentially and specifying the memory range;

a data register keeping the data information input from the test port;

a comparator comparing the data read out from the memory device based on the specification of the address counter with the data kept in the data register;

an agreement number counter outputting a releasing signal when the number of agreement of the data comes to the specific value; and

a logic gate turning on a switch when the releasing signal is output, independent of the state of security bit.

7. A semiconductor circuit according to claim 6 comprising

an address register setting the initial value based on the address information input from the test port.

8. A semiconductor circuit comprising: a memory device to store a control program and data;

a central processing unit to execute a specific process according to the program;

a test port to input and output test signals;

a switch to control on/off between the test port and the central processing unit; and

a security releasing means comparing the data input a test port with the data stored in a memory device and turning on a switch when the two data agree.